



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|-----------------------|---------------------|------------------|
| 10/074,114 | 02/11/2002 | Christopher F. Bussan | CS10856 | 8285 |

20280 7590 07/28/2004

MOTOROLA INC
600 NORTH US HIGHWAY 45
ROOM AS437
LIBERTYVILLE, IL 60048-5343

EXAMINER

ADDY, ANTHONY S

ART UNIT PAPER NUMBER

2681

DATE MAILED: 07/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/074,114

Applicant(s)

BUSSAN ET AL.

Examiner

Anthony S Addy

Art Unit

2681

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 February 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-11 and 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Yu et al., U.S. Patent Number 6,735,454, (hereafter Yu)

Regarding claim 1, Yu discloses a method of coordinating events (see col. 10, line 28 through col. 11, line 54 and Fig. 5; where an example of the event times that constitute a sleep cycle are shown) in a microprocessor-based electronic device (see col. 11, lines 28-30) having a sleep mode (see col. 3, lines 8-10) the method comprising the steps of determining a list of event times to perform associated operating system events that require exiting sleep mode and entering a wake-up period to perform the

event tasks (see col. 10, line 28 through col. 11, line 54 and Fig. 5; where an example of the events that constitute a sleep cycle are shown); establishing a timing of fixed events wherein the electronic device exits the sleep mode and enters a wake-up period to perform the fixed events (see col. 10, lines 1-12); and delaying the event time for at least one of the operating system events to align with a fixed event such that the electronic device utilizes one wake-up period to perform both of the at least one of the operating system event and the fixed event (see col. 4, lines 38-49). The delay of the event time for at least one of the operating system events is inherent, since by compensating for both frequency drift and timing off-sets, the active-mode clock is re-activated later in the sleep mode.

Regarding claim 2, Yu discloses all the limitations of claim 1. In addition, Yu teaches a step of defining accuracy values for each associated operating system event time (see col. 3, lines 20-23; where a technique proposed for timing errors inherent in low frequency, low power clock based signal generators is to adapt a length of each sleep period based upon a timing accuracy of a previous sleep period is disclosed), where the accuracy values define an acceptable delay to apply in the delaying step (see col. 3, lines 24-36; where it teaches the sleep duration is decreased or increased for the next sleep period, depending on whether the mobile station woke up late or early to perform an event. Thus a decrease or increase in sleep duration is parallel to an accuracy value being applied in the delaying step).

Regarding claim 3, Yu discloses all the limitations of claim 2. In addition, Yu teaches a delaying step including the substeps of: determining if any of the event times

are set to occur before the next fixed event (see col. 6, lines 44-48; where it is shown the active mode clock is activated sufficiently in advance of the next paging slot to permit warm-up of components of the mobile station such as the CDMA circuitry); adding, for those event times of the previous step, the event times plus their associated accuracy values to provide delayed event times (see col. 6, line 57 through col. 7, line 31; where an estimation unit including a memory register for compensating frequency drift and power variations is disclosed); calculating which of the operating system delayed event times occur earliest in time (see col. 8, lines 15-48; where a timing error calculation unit and a timing error adjustment unit is disclosed to delay the activation of the active-mode clock by an amount sufficient to compensate for the estimated timing error elapsed); and setting a wake-up time for the operating system at the delayed event time of the previous step (see col. 8, line 28-45; where an active-mode clock activation unit is disclosed to activate the active-mode clock when an enabling control signal is received from the frequency drift compensation unit and the off-set compensation unit).

Regarding claim 4, Yu discloses all the limitations of claim 3. In addition, Yu teaches further steps of placing the electronic device in sleep mode (see col. 8, line 54-col. 9, line 3); waking up the electronic device at the delayed event time set in the setting step (see col. 9, lines 3-5); running an associated task at the delayed event time (see col. 9, lines 5-8); and at the completion, of the running step, performing the substeps of: checking to see if any of the events have expired and performing those expired events (see col. 9, lines 8-11); scheduling the next event to occur (see col. 9,

lines 12-25) and shutting down components of the electronic device (see col. 9, lines 25-28; where power savings are achieved over devices, thus shutdown, which do not compensate for frequency drift)

Regarding claim 5, Yu discloses all the limitations of claim 4. In addition, Yu teaches a checking substep which includes checking to see if a powering down time after the task overlaps a powering up time for the next event, upon which the components of the electronic device are kept powered up until the next event (see col. 9, lines 29-64).

Regarding claim 6, Yu discloses all the limitations of claim 1. In addition Yu teaches a step of providing an operating system timer to time the operating system event times (see col. 3, lines 8-10).

Regarding claim 7, Yu discloses all the limitations of claim 1. In addition Yu teaches wherein the establishing step the fixed events are layer 1 communication events (see col. 3, lines 24-26; where a layer 1 communication event is interpreted to mean a modulation, or conversion between the representation of digital data in a user equipment and the corresponding signals transmitted over a communications channel) and the electronic device is a radiotelephone (see col. 1, lines 10-14).

Regarding claim 8, Yu discloses a method of coordinating events (see col. 10, line 28 through col. 11, line 54 and Fig. 5; where an example of the events that constitute a sleep cycle are shown) in a microprocessor-based communication device (see col. 11, lines 28-30) having a sleep mode (see col. 3, lines 8-10) the method comprising the steps of providing an operating system timer to time the operating

Art Unit: 2681

system event times (see col. 3, lines 8-10); determining a list of event times to perform associated operating system events that require exiting sleep mode and entering a wake-up period to perform the event tasks (see col. 10, line 28 through col. 11, line 54 and Fig. 5; where an example of the events that constitute a sleep cycle are shown); defining accuracy values for each associated operating system event time (see col. 3, lines 20-23; where a technique proposed for timing errors inherent in low frequency, low power clock based signal generators is to adapt a length of each sleep period based upon a timing accuracy of a previous sleep period is disclosed), where the accuracy values define an acceptable delay to apply in the delaying step (see col. 3, lines 24-36; where it teaches the sleep duration is decreased or increased for the next sleep period, depending on whether the mobile station woke up late or early to perform an event. Thus a decrease or increase in sleep duration is parallel to an accuracy value being applied in the delaying step); establishing a timing of communication events wherein the communication device exits the sleep mode and enters a wake-up period to perform the communication events (see col. 10, lines 1-12); and delaying the event time for at least one of the operating system events to align with a communication event such that the communication device utilizes one wake-up period to perform both of the at least one of the operating system event and the communication event (see col. 4, lines 38-49). The delay of the event time for at least one of the operating system events is inherent, since by compensating for both frequency drift and timing off-sets, the active-mode clock is re-activated later in the sleep mode.

Regarding claim 9. Yu discloses all the limitations of claim 8. In addition, Yu teaches a delaying step including the substeps of: determining if any of the event times are set to occur before the next communication event (see col. 6, lines 44-48; where it is shown the active mode clock is activated sufficiently in advance of the next paging slot to permit warm-up of components of the mobile station such as the CDMA circuitry); adding, for those event times of the previous step, the event times plus their associated accuracy values to provide delayed event times (see col. 6, line 57 through col. 7, line 31; where an estimation unit including a memory register for compensating frequency drift and power variations is disclosed); calculating which of the operating system delayed event times occur earliest in time (see col. 8, lines 15-48; where a timing error calculation unit and a timing error adjustment unit is disclosed to delay the activation of the active-mode clock by an amount sufficient to compensate for the estimated timing error elapsed); and setting a wake-up time for the operating system at the delayed event time of the previous step (see col. 8, line 28-45; where an active-mode clock activation unit is disclosed to activate the active-mode clock when an enabling control signal is received from the frequency drift compensation unit and the off-set compensation unit).

Regarding claim 10, Yu discloses all the limitations of claim 9. In addition, Yu teaches further steps of placing the communication device in sleep mode (see col. 8, line 54-col. 9, line 3); waking up the communication device at the delayed event time set in the setting step (see col. 9, lines 3-5); running an associated task at the delayed event time (see col. 9, lines 5-8); and at the completion, of the running step, performing

the substeps of: checking to see if any of the events have expired and performing those expired events (see col. 9, lines 8-11); scheduling the next event to occur (see col. 9, lines 12-25) and shutting down components of the communication device (see col. 9, lines 25-28; where power savings are achieved over devices, thus shutdown, which do not compensate for frequency drift).

Regarding claim 11, Yu teaches all the limitations of claim 10. In addition, Yu teaches a checking substep which includes checking to see if a powering down time after the task overlaps a powering up time for the next event, upon which the components of the communication device are kept powered up until the next event (see col. 9, lines 29-64).

Regarding claim 13, Yu discloses a method of coordinating events (see col. 10, line 28 through col. 11, line 54 and Fig. 5; where an example of the events that constitute a sleep cycle are shown) in a microprocessor-based communication device (see col. 11, lines 28-30) having a sleep mode (see col. 3, lines 8-10) the method comprising the steps of providing an operating system timer to time the operating system event times (see col. 3, lines 8-10); determining a list of event times to perform associated operating system events that require exiting sleep mode and entering a wake-up period to perform the event tasks (see col. 10, line 28 through col. 11, line 54 and Fig. 5; where an example of the events that constitute a sleep cycle are shown); defining accuracy values for each associated operating system event time (see col. 3, lines 20-23; where a technique proposed for timing errors inherent in low frequency, low power clock based signal generators is to adapt a length of each sleep period based

Art Unit: 2681

upon a timing accuracy of a previous sleep period is disclosed), where the accuracy values define an acceptable delay to apply in the delaying step (see col. 3, lines 24-36; where it teaches the sleep duration is decreased or increased for the next sleep period, depending on whether the mobile station woke up late or early to perform an event. Thus a decrease or increase in sleep duration is parallel to an accuracy value being applied in the delaying step); establishing a timing of communication events wherein the communication device exits the sleep mode and enters a wake-up period to perform the communication events (see col. 10, lines 1-12); adding, for those event times of the previous step, the event times plus their associated accuracy values to provide delayed event times (see col. 6, line 57 through col. 7, line 31; where an estimation unit including a memory register for compensating frequency drift and power variations is disclosed); calculating which of the operating system delayed event times occur earliest in time (see col. 8, lines 15-48; where a timing error calculation unit and a timing error adjustment unit is disclosed to delay the activation of the active-mode clock by an amount sufficient to compensate for the estimated timing error elapsed); and setting a wake-up period for the operating system at the delayed event time of the previous step (see col. 8, line 28-45; where an active-mode clock activation unit is disclosed to activate the active-mode clock when an enabling control signal is received from the frequency drift compensation unit and the off-set compensation unit) such that the communication device utilizes one wake-up period to perform both of the at least one of the operating system event and the communication event (see col. 4, lines 38-49). The delay of the event time for at least one of the operating system events is inherent, since

by compensating for both frequency drift and timing off-sets, the active-mode clock is re-activated later in the sleep mode.

Regarding claim 14, Yu teaches all the limitations of claim 13. In addition, Yu teaches further steps of placing the communication device in sleep mode (see col. 8, line 54-col. 9, line 3); waking up the communication device at the delayed event time set in the setting step (see col. 9, lines 3-5); running an associated task at the delayed event time (see col. 9, lines 5-8); and at the completion, of the running step, performing the substeps of: checking to see if any of the events have expired and performing those expired events (see col. 9, lines 8-11); scheduling the next event to occur (see col. 9, lines 12-25) and shutting down components of the communication device (see col. 9, lines 25-28; where power savings are achieved over devices, thus shutdown, which do not compensate for frequency drift).

Regarding claim 15, Yu teaches all the limitations of claim 14. In addition, , Yu teaches a checking substep which includes checking to see if a powering down time after the task overlaps a powering up time for the next event, upon which the components of the communication device are kept powered up until the next event (see col. 9, lines 29-64).

Claim Rejections - 35 USC § 103

3. Claims 12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yu et al., U.S. Patent Number 6,735,454, (hereafter Yu)** as applied to claims 8 and 13 above, and further in view of **Jokinen et al., U.S. Patent Number 5,416,435, (hereafter Jokinen)**

Regarding claims 12 and 16, Yu teaches all the limitations of claims 8 and 13. Yu does not teach a GSM operating system.

Jokinen, however, discloses a GSM operating system (see col. 3, lines 35-50) that can be used to save power in portable cellular phones, where the phone switches to a power saving mode at certain time intervals, but where time has to be measured accurately.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the GSM operating system as taught by Jokinen, for the mobile station of Yu to maintain system timing accuracy during the sleep and wake-up mode.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Storm et al., U.S. Patent Number 6,016,312 discloses a radiotelephone and method for clock calibration for slotted paging mode in a CDMA radiotelephone system.

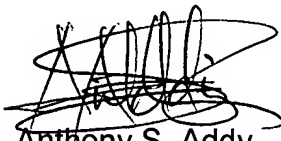
Shohara et al., U.S. Patent Number 6,473,607 discloses a communication device with a self-calibration sleep timer.

Roberts et al., U.S. Patent Number 6,212,398 discloses a wireless telephone that rapidly reacquires a timing reference from a wireless network after a sleep mode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony S Addy whose telephone number is 703-305-8487. The examiner can normally be reached on Mon-Fri 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David R Hudspeth can be reached on 703-308-4825. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Anthony S. Addy
July 21, 2004



ERIKA GARY
PATENT EXAMINER